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Pipelined ADC Digital Calibration by Using Polynomial Inverse Function

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Abstract*:* In this paper, a novel and simple digital technique to correct pipelined ADC errors is presented. The technique uses an inverse function for the entire ADC. Linearity of the ADC is improved by simultaneously adjusting the digital gain of the stages and the coefficients of the polynomials inverse function, using presented scheme. Output codes of the stages are applied to digital unit for calibration. Errors include capacitors mismatch, finite and nonlinear gain of Operational Amplifier (opamp), offset of opamp, and offset of sampling switches. The used algorithm is digital, completely. Trade-off between the speed and the accuracy of the pipelined ADC is improved by this technique, extensively. In the proposed technique, design problems of analogue circuits are moved inside digital circuit. The technique is simulated on a prototype 10bit 1.5bit/stage pipelined ADC with nonlinear opamp by using MATLAB/Simulink. After the proposed calibration, the ADC achieves 64.5 dB SNDR and 73dB SFDR which are restricted to 51.2 dB and 57dB respectively before calibration.

Keywords: component; pipelined ADC, digital calibration, polynomials inverse function

I. INTRODUCTION

Demand for high speed data conversion in multimedia applications is increased for mobile and fixed communications [1]. For example standard IEEE 802.16 which is used in cell phones and mobile networks requires ADCs with the sampling rate of 15 MHz to 250 MHz and the resolution of 10 to 16 bits [2], [3]. Pipelined ADCs are popular in high resolution and high speed applications. Therefore, research span of pipelined ADCs are concentrated in the techniques which increase the speed and reduce the power consumption [4].

Unfortunately by enhancement of resolution, power dissipation of pipelined ADCs increases due to the high gain requirements of opamps [2]. Also in sub-100nm technologies, power dissipation increases due to power supply reduction. This causes opamp gain decreases remarkably which influence design of high resolution and low power ADCs [5]. New researches on enhancement of battery life in mobile communications have led to the design of opamp with low gain and low accuracy [4] or replacement of opamps with low power circuits [6]. This leads to use digital calibration technique which relaxes design complexity of analog circuits [3].

In the proposed technique to calibrate the digital output, errors of all stages are eliminated simultaneously by adaptive algorithm. In this technique, analog circuits which exist in the path of the signal are not manipulated. Therefore, the speed of the ADC which depends on the process is not reduced. By using this technique, memory-less errors such as capacitors mismatch, charge injection, finite gain, nonlinearity of the gain, and finite bandwidth of opamps can be eliminated. Therefore, by the use of this technique we can reduce the power dissipation and increase the accuracy. The paper is organized as follows. Section II describes pipelined ADCs model. Section III details the proposed calibration technique. Section IV provides the simulation results for verification.

II. PIPELINED ADC MODEL

The architecture of a pipelined ADC is shown in Fig.1 which consists of a sample and hold and N pipelined stages. At the front end, the sample and hold circuit converts a continuous time input $V_{in}(t)$ into a sampled sequence $V_{in}[n] = V_{in}(nT_S)$ where T_S denotes the sampling period. The sampled analog input $V_{in}[n]$ is then digitized sequentially by passing it through N pipelined stages. In this block diagram the delays introduced by interstage latching are ignored [7]. As shown in Fig.1, each stage consists of a sub-ADC, a sub-DAC, and a residue amplifier with a gain of $g_{a,k}$. the output of the *k*th stage is given by

$$D_k[n] = V_{in,k}[n] + \varepsilon_{q,k}[n] \qquad (1)$$

where $V_{in,k}[n]$ is the Sub-ADC's input signal, and $\varepsilon_{q,k}[n]$ is the quantization error introduced by the Sub-ADC. If the Sub-ADC of stage k has a resolution of n bits then the magnitude of $\varepsilon_{q,k}[n]$ is bounded by $|V_{ref}/2^n|$. The ideal behavior of each Sub-DAC is to convert the format of its input from a digital representation to an analog representation without introducing distortion or noise [2]. The difference $V_{in,k}[n]$- $\varepsilon_{q,k}[n]$ is

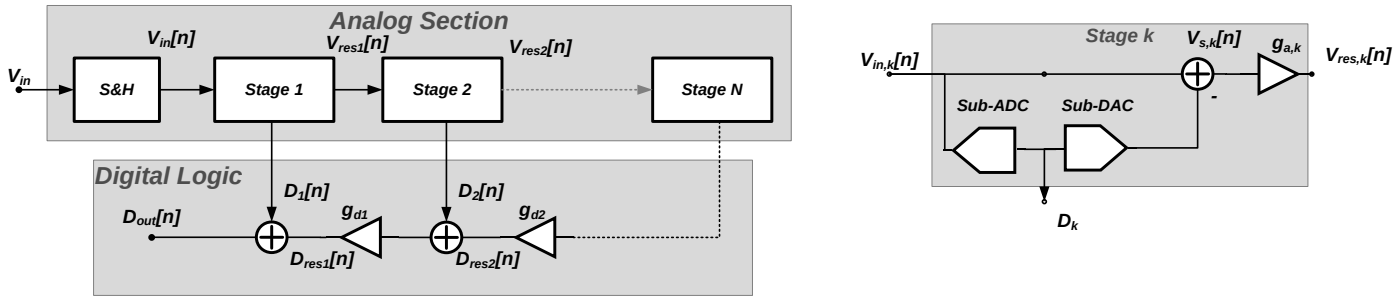

Figure 1. Pipelined ADC block diagram.

amplified by $g_{a,k}$ and transferred to the next stage[7]. The input and output of the *k*th residue amplifier at the nth sample time are given, respectively, by

$$V_{d,k}[n] = -\varepsilon_{q,k}[n]$$
$$V_{res,k}[n] = g_{a,k}\varepsilon_{q,k}[n] \quad (2)$$

The output of each stage is bounded by $|\varepsilon_{q,k}[n]_{max} g_{a,k}|$. When stage k has a resolution of the n_i bits then $g_{a,k}$ must be 2^{ni}. If the sub-ADC of *k*th stage has a resolution of n_r bits then $\varepsilon_{q,k}[n]$ is bounded by $|V_{ref}/2^{nr}|$. In this case the output of the *k*th stage ($V_{in,k}[n]$) is bounded by $|V_{ref}/2^{nr-ni}|$.

With ideal circuit behavior, the magnitude of the quantization error from each Sub-ADC is bounded by $\varepsilon_{q,k}$, so the analog output of each pipeline stage ideally never exceeds $g_{a,k}.\varepsilon_{q,k}$ in magnitude. However, nonideal circuit behavior such as comparator offset voltages can cause the analog outputs of the pipeline stages to have magnitudes that exceed from time to time. To accommodate such over-range conditions, n_r must be greater than n_i ($n_r > n_i$), in this case the pipelined ADC is said to have over-range margin of $V_{ref}(1\text{-}1/2^{nr-ni})$. When $n_r = n_i$ in this case the pipelined ADC doesn't have any over-range margin [7]. The over-range margin greatly relaxes the performance requirements of the sub- ADCs in pipelined ADCs [2].

The outputs of the Sub-ADCs are combined as shown in Fig. 1 to form the output of the pipelined ADC, D_{out}. The output of each digital gain ($g_{d,k}$) $D_{res,k}$ which is called the digitized residue of the kth stage is as follows:

$$D_{res,k}[n] = g_{d,k}\left(D_{res,k+1}[n] + D_{k+1}[n]\right) \quad (3)$$

Hence, in the absence of nonideal circuit behavior the quantization error sequences from all but the last pipeline stage cancel to give

$$D_{out}[n] = V_{in}[n] + \prod_{k=1}^{N-1} g_{d,k}\varepsilon_{q,N}[n] \quad (4)$$

The second term in (4) is the quantization error of the pipelined ADC, which is the quantization of the last stage ($\varepsilon_N[n]$) multiplied by all the previous digital gains.

A. The signal to noise ratio (SNR)

When the last stage has a resolution of B_N bits then the magnitude of $\varepsilon_{q,N}$ is bounded by $V_{ref}/2^{BN}$. In this case by using (4), SNR can be written as follows[8]:

$$SNR = 20\log\left(\prod_{k=1}^{N-1} g_{d,k}\right) + 1.76dB \quad (5)$$

III. THE PROPOSED DIGITAL CALIBRATION

In this section, the proposed calibration scheme which uses the polynomials inverse function is presented. The proposed scheme uses an inverse function for the entire ADC, which is placed at the digital output of the ADC. Although the proposed calibration technique is simpler than other nonlinear calibration techniques, which uses inverse function for first few stages, has better performance in cost of convergence time. This work uses the presented techniques in [3] and [6] and improves them. The digital output of an ideal ADC (D_{ADC}), which is the desired digital output of the ADC, is the quantized version of the input voltage ($V_{in,ADC}$).

Though in the ideal ADC, the digital output depend on the input linearly, Sampling capacitors mismatches, finite and nonlinear gain cause distortion in ADC. Therefore, digital output without calibration ($D_{out,ADC}$) in the ADC have sectional curves which cause nonmonotonicity, missing codes and hysteresis effect [6]. Fig. 3 shows the transfer function of a real

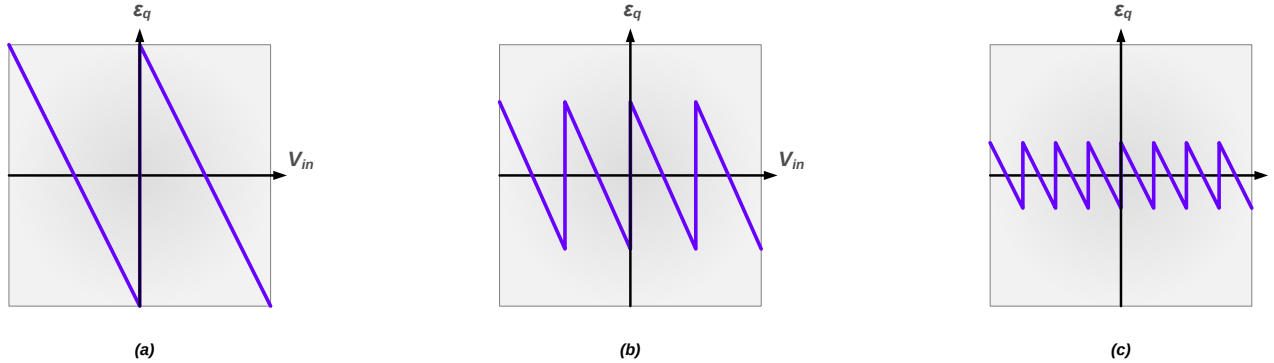

Figure 2. Ideal residue plot with (a) nr = ni, (b) nr = ni+1, (c) nr = ni+1.

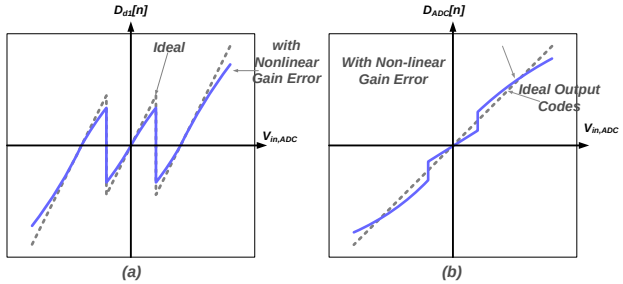

Figure 3. The effect of nonlinearity: (a) the first stage output voltage ,(b) ADC output codes

pipelined ADC before error calibration.

Pipelined ADC which suffers from different errors can be modelled as $D_{out}=f(V_{in,ADC})$. The inverse function $(f(x)^{-1})$ in digital domain can eliminate all of errors which exist in the output of the ADC, But the digital output is sectional which makes difficult implementation of such digital circuits [3].

For simplicity, only the effect of the first stage of the pipelined analog to digital converter output codes is considered. Fig. 4 shows an alternative representation of the ADC stage that is well-suited for further analysis. The sub-ADC has been modeled as a summing node which adds the quantization error and Sub-DAC has been replaced by a wire. The digital output of the first stage can be written as follows:

$$D_1 = V_{in,ADC}[n] + \varepsilon_{q1}[n] \tag{6}$$

The rest of the stages are considered ideal as shown in Fig. 4. The input voltage and output characteristics of backend ADC can be written as follows:

$$D_{res1}[n] = V_{res1}[n] + \varepsilon_{be}[n] \tag{7}$$

where V_{res1} is the output voltage of the first stage and $D_{res,1}$ is the digital output of the ideal backend ADC. ε_{be} is the ideal quantization error of the backend ADC. The digital output is written as follows:

$$D_{ADC}[n] = D_1[n] + \varepsilon_{q1}[n] + g_{d1}\left(g_{a1}(V_{d1}[n]) + \varepsilon_{be}\right) \tag{8}$$

where D_1 is the digital output of the first stage; ε_{q1} is the quantization error of the first stage. In equation (7), the effect of the first stage's quantization error is as follows:

$$e(\varepsilon_{q1}[n]) = \varepsilon_{q1}[n] + g_{d1}\left(g_{a1}(-\varepsilon_{q1}[n])\right) \tag{9}$$

When the first stage has nonlinear error, by changing the digital gain of the first stage g_{d1}, $e(\varepsilon_{q1})$ is not eliminated for the entire input voltage range. But by using the least mean square algorithms, at a specified digital gain $g_{d1\text{-}opt\text{-}lin}$, $e(\varepsilon_{q1})$ for the entire input voltage range reduced to a minimum.

The proposed method uses the inverse function of the ADC to eliminate gain error of stages. As described in [6], due to monotonic codes caused by the gain error, the inverse function can not be used. As shown in Fig. 3(a), the peaks of $e(\varepsilon_{q1})$ are on the edges of the Sub-ADC's decision which are discontinuous. The peaks result in missing codes in the ADC's digital output, as shown in Fig. 3(b). Thus creating inverse function is very difficult and impractical.

With a specified value of digital gain g_{d1}, $e(\varepsilon_{q1})$ on the edges of the Sub-ADC's decision is corrected which is shown by $g_{d1\text{-}opt\text{-}nonlin}$. By $g_{d1\text{-}opt\text{-}nonlin}$, missing codes can be eliminated

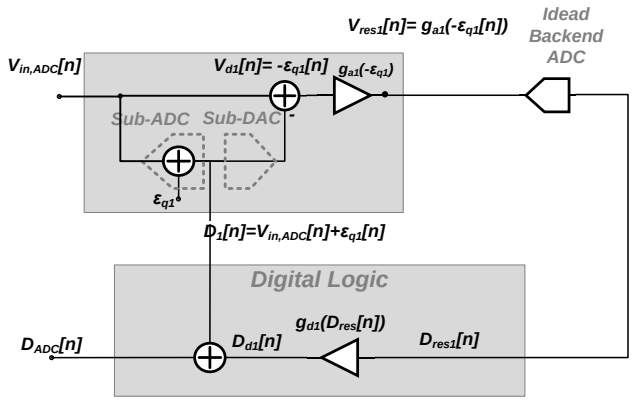

Figure 4. Calibration Structure

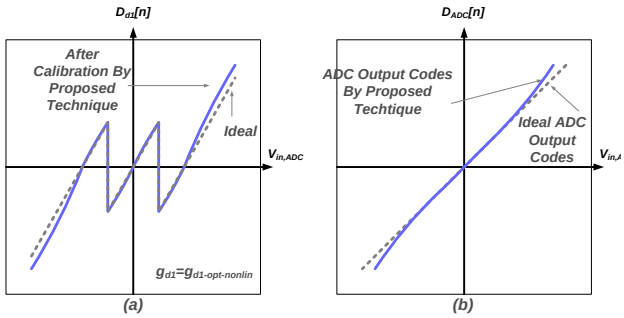

Figure 5. The effect of nonlinearity by proposed calibration: (a) the first stage output voltage ,(b) ADC output codes.

and the discontinuity of $e(\varepsilon_{q1})$ is eliminated for the entire input voltage range as shown in Fig. 5(a). The ADC's digital output is shown by D_{raw} as shown in Fig. 5(b). Inverse function is used by the proposed technique to correct D_{raw}.

The ADC's calibrated digital output, $D_{ADC,cal}$ are the function of D_{raw} as shown in Fig.6. D_{raw} can be approximated by using polynomials:

$$D_{\mathrm{ADC,cal}}[n] = g^{-1}(D_{\mathrm{raw}}[n]) \approx \sum_{k=1}^{M} a_k D^{k}{}_{\mathrm{raw}}[n] \tag{10}$$

Equation (10) represents a polynomial with the coefficients of a_k, as a function of D_{raw}. If the digital gain of the first stage g_{d1} is adjusted with the coefficients of the polynomials inverse function simultaneously, the digital gain of the first stage is adjusted to $g_{d1\text{-}opt\text{-}nonlin}$ and the given problem in [6] will be prevented. By expanding nonlinear gains to all stages, equation (8) can be written as follows:

$$D_{raw}[n] = V_{in}[n] + \prod_{j=1}^{N-1} g_{d,j}\varepsilon_{qN}[n] + error[n]$$

$$error[n] = e(\varepsilon_{q1}[n]) + g_{d,1}e(\varepsilon_{q2}[n]) + \ldots + \prod_{j=1}^{N-2} g_{d,j}e(\varepsilon_{qN-1}[n]) \tag{11}$$

According to equation (11), it can be deduced that the nonlinearity effects of the first stages influence the nonlinearity of the total digital output D_{raw} more than last stages.

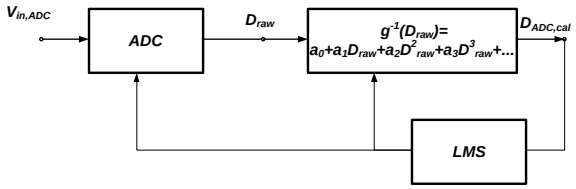

Figure 6. Proposed Calibration Structure by using polynomial inverse function.

A. The proposed magnification

As it is given in equation (10), in the approximated polynomials inverse function, the calibrated output by the proposed technique ($D_{ADC,cal}$) is summations of the powered inputs. Every term in equation (10) lowers by the enhancement of the power in the polynomials because of D_{raw}<1. To use efficiently the polynomials inverse function and to have less bits in practical implementations, magnification factor (S) is used and $D_{ADC,cal}$ is defined as:

$$D_{\mathrm{ADC,cal}}[n] = g^{-1}(D_{\mathrm{raw}}[n]) \approx \sum_{k=1}^{M} a_k S^k D^k{}_{\mathrm{raw}}[n] \quad (12)$$

If S is not used, the terms with the greater power than 3 will become so small. In the foreground digital calibration to relax the circuit implementations, the magnification factor (S) is approximated.

B. Adjusting the weights of stages and the polynomial coefficients

A Least-Mean-Square (LMS) algorithm is used for adjusting the weight of the stages, the polynomial coefficients and the proposed magnification factor (S). LMS Algorithm adjusts them by using an specified input values ($V_{in,ADC}$) and desired output (D_{ADC}). LMS is an iterative algorithm which needs to be repeated until the weights become adjusted [9]. The weights and coefficients are extracted as follows:

$$\begin{aligned} a_k[n+1] &= a_k[n] + \eta e S^k D^k{}_{raw} \\ g_k[n+1] &= g_k[n] + \eta e D_k \sum_{i=1}^{N} i a_i S^i D^{i-1}{}_{raw} \\ S[n+1] &= S[n] + \eta e D_k \sum_{i=1}^{N} i a_i S^{i-1} D^i{}_{raw} \\ e &= D_{ADC} - D_{ADC,cal} \end{aligned} \quad (13)$$

In equations (13), e is the difference between the desired output and the calibrated output codes by polynomial inverse function. η is the update step-size in *LMS* which have to be between 0< η <1.

IV. Simulation Results

The proposed technique was simulated using MATLAB/Simulink. In these simulations, to achieve the 10-bit accuracy, a 14-stage inaccurate pipelined ADC is used. A 14-bit ideal pipelined ADC is necessary to calibrate the inaccurate ADC. The gain of the opamps in the stages is ten (A=10). The nonlinearity factor is defined as follows:

$$V_{\mathrm{out}} = f(V_{\mathrm{in}}) = \left(\frac{A(V_{\mathrm{in}})}{1 + A(V_{\mathrm{in}})/2}\right) V_{\mathrm{in}}$$
$$A(V_{\mathrm{in}}) = A(1 - 0.25 V_{\mathrm{in}}{}^2) \quad (13)$$

The offset for the stages opamp is assumed 25mV. For the inverse function of polynomials, the order is chosen 3. The

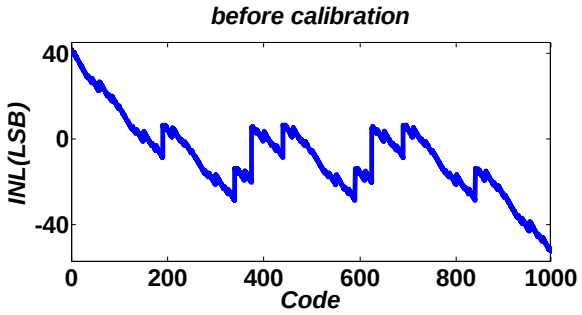

Figure 7. Simulated INL before calibration.

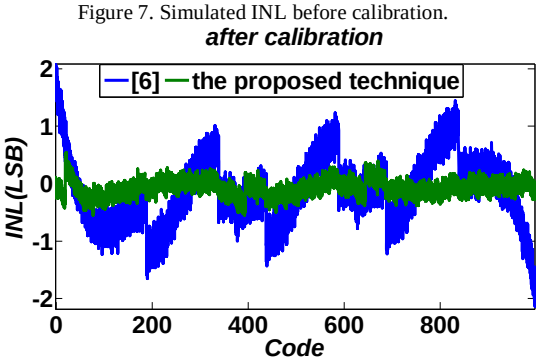

Figure 8. Simulated differential and integral nonlinearity after calibration by the proposed technique and the technique used in [6].

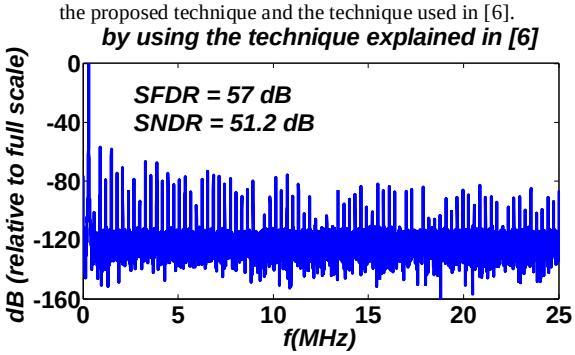

Figure 9. Output spectrum after calibration by [6] for 485 KHz input frequency and 50-MHz sampling rate.

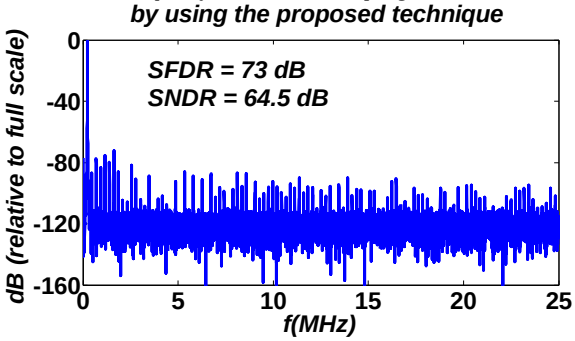

Figure 10. Output spectrum after calibration by the proposed technique for 485 KHz input frequency and 50-MHz sampling rate.

TABLE I. Comparison of the proposed technique and the technique explained in [6].

	SFDR	SNDR	INL
The Proposed technique	73 dB	64.5 dB	0.5 LSB
The technique explained in [6]	57 dB	51.2 dB	2 LSB

uncalibrated ADC suffers from a large number of missing codes and an INL of 50 LSB.

By using the proposed technique, the ADC achieves 0.5 LSB INL, 64.5 dB SNDR and 73dB SFDR which are restricted to 2 LSB INL, 51.2 dB SNDR and SFDR 57dB respectively by the technique explained in [6]. Thanks to the proposed technique, the total accuracy of the ADC is improved about 2 bits in comparison with the technique explained in [6] and the inaccurate ADC is corrected up to 10-bit.

Table I shows simulation results by using both the proposed technique and the technique explained in [6]. Fig. 7 shows the simulated integral nonlinearity of the ADC before calibration. Fig. 8 shows the simulated integral nonlinearity of the ADC after calibration by the proposed technique and the technique used in [6]. Fig. 9 shows the output spectrum of the ADC after calibration by the used technique in [6]. Fig. 10 shows the output spectrum of the ADC after calibration using the proposed technique.

CONCLUSION

In this paper a proposed digital calibration technique is presented to eliminate the linear errors of 1.5bit/stage pipelined ADCs produced by the finite and nonlinear gain in stages opamps. The effectiveness of the proposed technique is demonstrated. The proposed technique improves nonlinearity errors of the stages, better than other techniques. In this technique, analog circuits which exist in the path of the signal are not manipulated.

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