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# Design and Implementation of an Advanced Digital Communication System Based on SDR

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**Abstract:** Modern digital communication systems require simplicity, flexibility, and high scalability. This can be achieved using software-defined radio (SDR) technology, which depends on digital signal processing (DSP) software algorithms. This paper considers designing the modulation and the demodulation parts of a single carrier digital communication system based on a microcontroller ($\mu$C), in which the signal is modulated digitally using a look-up table (LUT) module. Meanwhile, the receiver demodulates the signal using a digital signal processing algorithm by utilizing a single carrier discrete Fourier transform (DFT), both the receiver and transmitter employ a Teensy 4.0 microcontroller which can be programmed using C++ language. The target data rate used as a test for this paper is 10 Kilo symbols/sec (KS/s), which will support multi-modulation types. Modulation schemes such as BPSK, QPSK, 8QAM, 8PSK, and 16QAM are generated for the transmitter. At the same time, at the receiver, the symbols phases are exploited to detect the signal, rather than the amplitude and this method is suitable for any modulation schemes, as summary in this paper will achieve the design of two new ideas first is to modulate the signal using $\mu$C and the other is the method of demodulate the signal using the $\mu$C.

**Keywords:** Digital modulation, microcontroller, software-defined radio (SDR), C++, Mary phase shift keying (MPSK), and M-ary Quadrature amplitude modulation (MQAM).

## 1. INTRODUCTION

Digital modulation technologies play a significant role in modern communication systems. In recent years, the world has seen a huge expansion in this field, in which digital modulation has taken the place of analog modulation types in several communication systems. Therefore, a wide development in the field of digital communication has been achieved. The world has witnessed, during the last decade, a large industrial revolution in microprocessors and digital signal processing (DSP) algorithms, which makes the microprocessor more suitable to be employed in the field of DSP and most digital communication systems. Nowadays, flexibility and scalability become prerequisites in modern communication systems. This is because of the new bands of spectrum and the evolution of communication systems. For these reasons, communication systems become dependent on a fixable software system named software-defined radio (SDR) technology, which is employed for modulation and demodulation with the assistance of the DSP algorithms. In the past, these techniques were fixed with unique circuits for every modulation system. These technologies paved the road to developing an updated modern digital communication system [1]. In the SDR system, data is processed in a microprocessor and modulated digitally, then it is sent to a digital-to-analog converter (DAC) circuit to obtain the modulated signal. The latter is sent then to the RF component to be transmitted. On the receiver side, the received signal is converted to digital using an analog-to-digital converter (ADC), which achieves processing using DSP in the microprocessor to demodulate the signal [1], [2], [3].

Furthermore, there are various SDR architectures and topologies. Some topologies depend on their work on Field programmable gate array (FPGA). While the general purpose processor (GPP) is considered the principle of other techniques. Moreover, the two topologies are merged on some SDR to obtain the advantage of GPP and FPGA. The choice of which method is employed depends on different parameters such as the speed, the price, and the SDR working environment [4] and [5]. The aim goals of this paper are emphasized by implementing the modulation and demodulation stages by applying these topologies.

A real-time modulation scheme based on an FPGA for digital communication has been designed and implemented in [6], [7], [8], in which the FPGA is programmed by utilizing VHDL language for the sake of obtaining higher

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performance with simpler confirmation. The disadvantages of the FPGA can be summarized as lower flexibility and harder to implement than the GPP [1]. In this paper, the aim is to investigate the ability and the difficulties of designing a special digital modulation system using a microcontroller and attempt to implement the design. The microprocessor is utilized by using a clock of 600MHz with speed CORTEX M7, which is built in the MIMXRT1062 microcontroller chip, which is used then by the Teensy 4.0 microcontroller programming board [9]. The board can be programmed using C++ language and Arduino IED. This microcontroller has been chosen because the clock speed is suitable for the DSP field, and its cost is low compared to other microcontrollers, also it has been used in the digital modulation field [10].

In this context, the transmitter and receiver's functions and implementation via SDR are provided in [11], in which single-board computers with low-cost SDR devices are used for spectrum visualization for frequency modulation (FM) band. Moreover, SDR transceivers are examined using GNU radio software in [12], [13]. In [14] cognitive SDR has been proposed for automatically recognizing different types of signals via exploiting an architecture consisting of a convolution neural network (CNN). Besides, the SDR is merged with configurable radio frequency (RF) and Field Programmable Gate Array (FPGA) devices in [15] for different digital operation purposes for communication systems. Additionally, SDR is utilized to design QPSK modulation scheme in [16], in which the SDR is used to govern the digital signal processing of the designed systems' devices such as the filter, mixer, modulator, and demodulate. Different signal processing approaches for several digital communication systems are introduced and realized in [17], [18], [19], [20] by using SDR.

The main contribution of this paper is the design and implementation of multi-real-time modulation types transmitters and the real-time demodulation of a single carrier by utilizing Teensy 4.0 $\mu$C and DSP algorithms. The signal can be digitally modulated in different modulation schemes at the transmitter by utilizing a look-up table (LUT) module that stores all possible symbols for any modulation scheme in the microcontroller. On the other hand at the receiver, a digital signal processing algorithm, via utilizing a single carrier discrete Fourier transform (DFT), has been proposed and implemented. The detection by using the proposed method relies on phase detection of the symbols rather than the conventional amplitude detection. For perfect detection of the transmitted signal, synchronization, guard delay, and sensing methods are proposed to avoid interference.

The paper is organized as follows; the theoretical background of different modulation schemes are discussed in Section 2. The software defined radio (SDR) is introduced and detailed in Section 3. Moreover, the implementation of the designed transmitter and receiver of the proposed system is explained and analyzed in Section 4. The results analysis is demonstrated in Section 5. Finally, we summarized the most outcomes and conclusions along with the proposed future works in Section 6.

## 2. Digital modulation

### A. Binary Phase shift keying (BPSK) Scheme

BPSK is used to send one bit in every symbol with two-phase probabilities, one phase for high level and another for low with differences of $180^o$. The mathematical expression can be defined for bipolar data bits as:

$$s_{BPSK}(t) = B(t)\cos(w_C t), \tag{1}$$

where B(t) is the data bits in bipolar form $\{1, -1\}$ and $w_C$ is the radio frequency of the carrier. The BPSK has the lowest symbol error rate (SER) among all other digital modulation schemes because it has only two phases [21], therefore, it is suitable for testing, the most well-known digital communication system that uses PSK modulation is the Global Positioning System (GPS) [22]. The consumed bandwidth for the BPSK is twice the bit rate which is higher than other M-ary PSK schemes. However, when the $\mu$C starts, the two symbols are calculated and stored in the random access memory (RAM). This process occurs once, i.e. there is no need to calculate the signal for every symbol.

### B. Quadrature PSK (QPSK) Scheme

QPSK transfers two bits per symbol with four-phase probabilities which can send the same bit rate of PSK with half symbol rate. This means it uses the half BW of PSK, the standard four-phase that QPSK uses is $45^o$, $135^o$, ($225^o$ or $-135^o$), ($315^o$ or $-45^o$). The QPSK waveform can be generated by taking two-bit every symbol and multiplying the first bit with a local oscillator, i.e. a single-tone sinusoidal signal, while the second bit is multiplied with the same sinusoidal signal but with $90^o$ phase shift. The two branched of the two bits are then summed to obtain the final QPSK waveform. Table. I explains the final results of the QPSK transmitter circuit.

in which the bits are in a bipolar form and B0(t), and B1(t) are utilized to control the phases in the in-phase (I) and quadrature-phase (Q) branches, respectively. This expression is employed to form the symbols for the four cases, which are stored in the RAM according to the bits at the input. Moreover, the mathematical expression for this

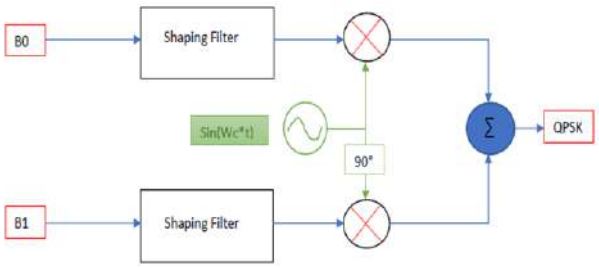


Figure 1. QPSK transmitter.

TABLE I. Input-output of the QPSK transmitter.

| Bit0 ($B_0$) | Bit1 ($B_1$) | $a = B_0 \sin(\theta)$ | $b = B_1 \sin(\theta + 90^o)$ | $a + b$ | Amp. |
|---|---|---|---|---|---|
| -1 | -1 | $180^o$ | $270^o$ | $225^o$ | $\sqrt{2}$ |
| 1 | -1 | $0^o$ | $270^o$ | $315^o$ | $\sqrt{2}$ |
| -1 | 1 | $180^o$ | $90^o$ | $135^o$ | $\sqrt{2}$ |
| 1 | 1 | $0^o$ | $90^o$ | $45^o$ | $\sqrt{2}$ |

modulation scheme can be written as

$$s_{QPSK}(t) = B0(t)\sin(w_C t) + B1(t)\cos(w_C t), \qquad (2)$$

At the receiver, the incoming signal is multiplied coherently, in two branches as well, one by $sin(\theta)$, and the other by $sin(\theta + 90^o)$. At the output of the two mixers, the signals are filtered by passing through a low pass filter (LPF), and the signals at the output of the filter represent the values at the I and Q branches, which are compared with a reference voltage to decide the logic in each branch as shown in Figure 2. It is noteworthy that the most well-known communication system that uses the QPSK modulation is the Digital Video Broadcasting–Satellite (DVB-S) and DVB-S2 [23], [24].

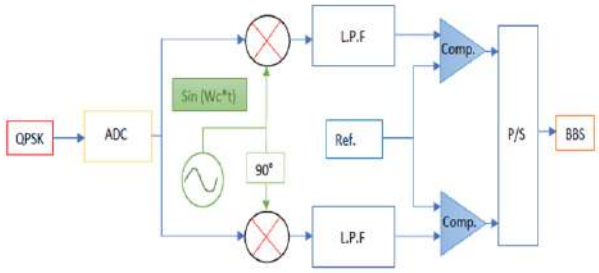


Figure 2. QPSK receiver.

### C. 8PSK

8PSK modulation scheme is employed to send 3 bits per symbol, which means that it can send triple the data rate compared to the BPSK over the same bandwidth. This modulation scheme has 8 potential phases with differences of $360^o/8 = 45^o$ between any two successive symbols. There are two common constellation diagrams for the 8PSK, the first has 8 symbols with a $45^o$ between each other, i.e. $22.5^o, 67.5^o, 112.5^o, 157.5^o$ , while the other constellation diagram starts from $0^o$ and ends at $180^o$ [25], [26]. However, every type has its own I and Q values table that produces the signal with the required phase. At the receiver and after the multiplication stage, i.e. the mixer stage, the output has multiple levels of voltages for the values in the I and Q branches. To decode these values for obtaining the original data bits, compactors for every side must be used with a logic circuit or ADC can be also utilized. In this paper, all the demodulation stages and the signal processing are implemented by a block of codes. Moreover, the most well-known communication system that uses the 8PSK modulation, is the DVB-S2 [24].

### D. QAM

Quadrature Amplitude Modulation (QAM) sends the signal with a variation of amplitudes and phases. This scheme is used wildly in most modern digital communication systems because it can send a high number of bits per symbol with better BER compared to MPSK, the most well-known communication system that uses the QAM is the wireless local area network protocol for the Wi-Fi standards [27]. The higher well-known order that has been used of QAM is 4096 [28], which means that it can transfer up to 12 bits per symbol, QAM needs a linear power amplifier (PA) because it uses multiple levels of amplitude for amplification, rather than the nonlinear one which it is more efficient than linear PA. To overcome this problem, APSK (Amplitude and phase-shift keying) modulation can be used instead. The latter utilizes phase and amplitude for modulation with lower levels of amplitude [29]. In this paper, the 8QAM and 16QAM are considered for transmission.

### E. 8QAM

The 8QAM is usually used in optical communication [30], [31], and there are many designs of constellation diagrams as shown in Figure 3. The square constellation diagram that is shown in Figure 3 (e) has been chosen for transmission. The symbols' phases demonstrate the same phases that the 8PSK. From the properties of the square, we can conclude that the four points that are in the corners of the square have an amplitude of 1.41 volts higher than the other four points. However, the 8QAM is considered better than 8PSK by 1 dB.

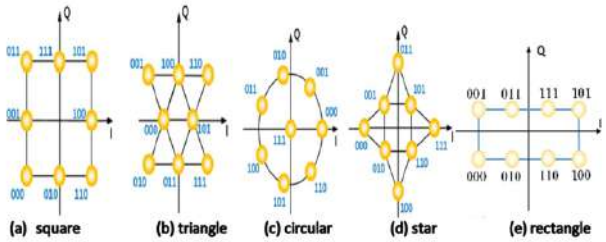


Figure 3. Different constellation diagrams for 8QAM modulation scheme [31], [32], [33].

*F. 16QAM*

16QAM sends 4 bits per symbol with 12 probable phases and three amplitude levels as shown in Figure 4, which shows the constellation diagram and the time domain signal of this modulation scheme As mentioned earlier,

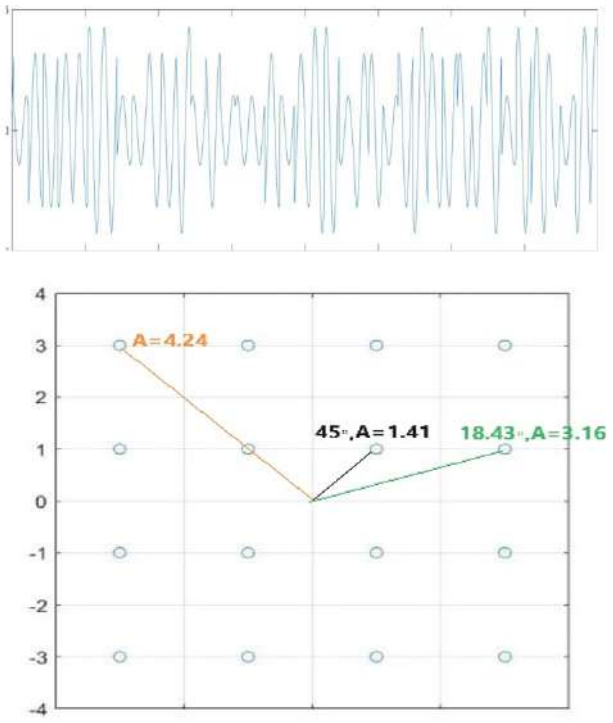


Figure 4. 16QAM time domain at the top, and the constellation diagram at the bottom.

there are three amplitude levels for the 16QAM signal which are 1.41, 3.16, and 4.24. Additionally,there are 12 phases $18.43^o$, $45^o$, $63.43^o$, $108.43^o$, $135^o$, $153.43^o$, $180^o$, $-18.43^o$, $-45^o$, $-63.43^o$, $-108.43^o$, $-135^o$, and $-153.43^o$. Moreover, 16QAM is employed in different communications systems like Digital Video Broadcasting – Terrestrial (DVB-T), Wi-Fi 802.11n standard, and Digital Subscriber Line (DSL) [34], [35], [36]. Furthermore, 16QAM has higher bandwidth efficiency than other previous schemes, because it can transfer four times of data rate of the PSK with the same bandwidth. For the design implemented in this paper for the transmitter, the 16 possible waves of the 16QAM are generated and stored in the $\mu$C.

## 3. SDR

Most modern communication systems rely on SDR technology which can offer flexibility and low cost. The main idea is that the signal is converted to digital form by using DAC and then the signal using DSP. The SDR receiver may contain an analog down-converter RF stage before the DSP processing, this stage may be not exited in some models which employ direct sampling instead. SDR provides maximum flexibility for the digital communication system especially when it uses GPP, because it allows the same hardware to be employed with different air interface standers, and the system can be easily updated by only updating the software part [37]. One example of an SDR system is a general-purpose SDR type like an RTL dongle receiver which can be used for researching and analyzing the frequency spectrum. Moreover, SDR can be combined with artificial intelligence (AI) for signal processing purposes, offering innovative solutions for improved intelligence gathering and analysis, with significant current capabilities and potential future advancements [38], [39], [40]. At the transmitter, the data can be modulated digitally and delivered to DAC to convert it to a real signal, the modulated signal is then passed to the RF component to be ready for transmission.

## 4. DESIGN IMPLEMENTATION

*A. Transmitter*

To produce the modulated signal using the microcontroller, a DAC circuit must be used. The R-2R ladder DAC circuit has been chosen for this purpose due to its simplicity with suitable performance without needing a complex filter circuit, and R-2R content of only resistors, the design is shown in Figure 5. The R-2R is a parallel DAC, and in

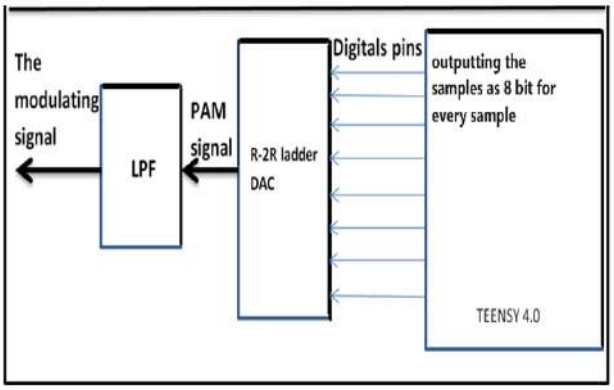


Figure 5. R-2R DAC

this design, it works with an 8-bit resolution for every sample which means that the step level is 1/255 volts, and the output of the DAC will be in the zero-order hold (ZoH) signal. The samples of the signal are generated and stored digitally in unsigned char arrays form as a look-up table (LUT) module inside the microcontroller for every modulation type, and to make it faster ; every bit of the 8 bits samples are stored as 1 byte char, so it can use with less processing. Each symbol has 25 samples as assumed in this paper, so it is easier to shape the signal using the LPF. The frequency, or symbol rate, can be controlled by controlling the delay between the samples, $\tau_D$, which can be calculated as follows:

$$\tau_D = \frac{T_{sy}}{N_s}, \tag{3}$$

where $T_{sy}$ is the duration of the required symbol rate and $N_s$ is the number of samples. There are several approaches to

produce the delay for the $\mu$C, but the most accurate method is to use the clock counter number inside the Teensy, which every clock cycle needs

$$\frac{1}{600MHz} = 1.67ns, \tag{4}$$

where 600 MHz represents the clock speed. As a result of the first try on the breadboard, 10 Kilo symbols per second (KS/s) of different modulation signals are modulated successfully with high resolution in real-time as shown in Figure 6. This figure contains a collection of the results for the multi-modulation signals in time domain using the oscilloscope in the laboratory. It is noteworthy that all modulations are based on a sin signal, not a cos. In other words, 90-degree rotation has been utilized for the Fourier transform, since the phase can be represented easier for the sin signal as it is started from 0 degrees. Besides,

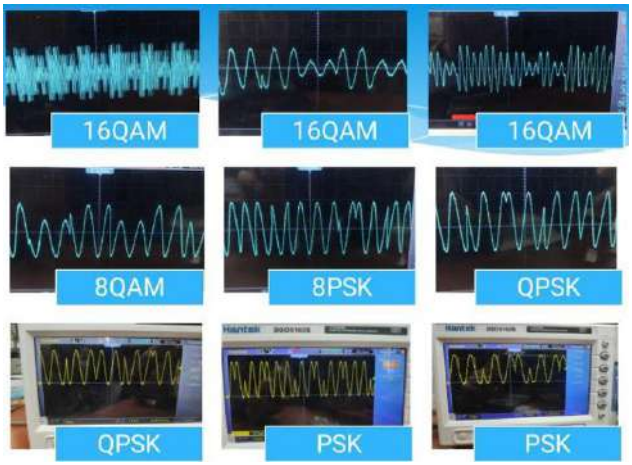


Figure 6. Signals Produced at the Transmitter.

the FFT property is used to evaluate the bandwidths of designed modulation schemes, i.e. the math option of the oscilloscope is utilized for this purpose. Moreover, the obtained results are perfectly matched with the theoretical formulas for bandwidth measuring. However, by sending the same symbol rate, i.e. 10KS/s, by using a different modulation scheme, the bandwidth is always the same, for that reason different symbol rates can be obtained. Figure 7 shows the bandwidth needed to transmit 10Kbps using PSK and QPSK modulation. It can be noticed that for a PSK with 10KS/s, the bandwidth is equal to 20 KHz, while for the QPSK with 5 KS/s, the bandwidth is 10KHz. The filtering circuit for the signal has been easily designed, that has a smooth signal at its output with simple first-order LPF. This is because of the high number of samples per symbol that have been used. Figure 8 shows the effect of the designed filter for different signal shapes for PSK modulation before and after the low pass filter. After obtaining the results on a Vero board. a PCB board has been designed for the transmitter circuit to make it more suitable for the testing environment as shown in Figure 9. From this figure, it can be noticed that additional components have been added in

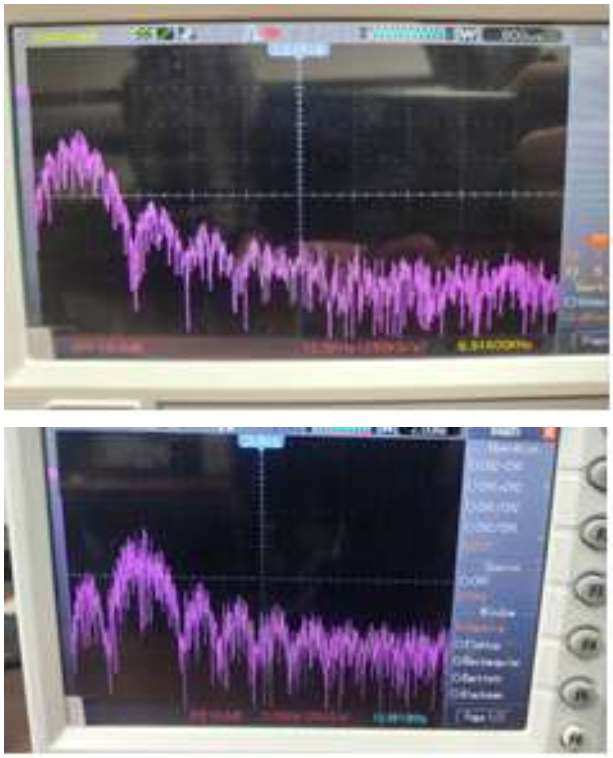

Figure 7. Spectrum of PSK at the top, and the spectrum of QPSK at the bottom.

addition to the $\mu$C and DAC, such as LEDs and switches for the selection of the required modulation scheme, and some serial peripheral interface (SPI) to make the measurement and testing of the designed system more convenient. The maximum symbol rate obtained for the 25 samples per symbol using the Teensy is about 400KS/s.

### *B. The Receiver*

In this paper and tt the receiver terminal, Teensy $\mu$C has been designed to process four samples per symbol, in which a fixed delay between samples is assumed from the analog-digital modulation signal. This can be achieved using the internal ADC with 8 bits as a resolution as shown in Figure 10, and the delay can be calculated as

$$T_s = \frac{T_{sy}}{4} - T_{DAC}, \tag{5}$$

Moreover, the four samples for every symbol must be processed using single carrier DFT (SC-DFT) as the following

$$DFT = \sum_{n=0}^{N-1} S(n) \cdot e^{-i\frac{2\pi kn}{N}} \tag{6}$$

Therefore, for a single carrier that contains 4 samples, (6) can be expressed as

$$DFT = \sum_{n=0}^{3} S(n) \cdot e^{-i\frac{2\pi kn}{4}}, \tag{7}$$

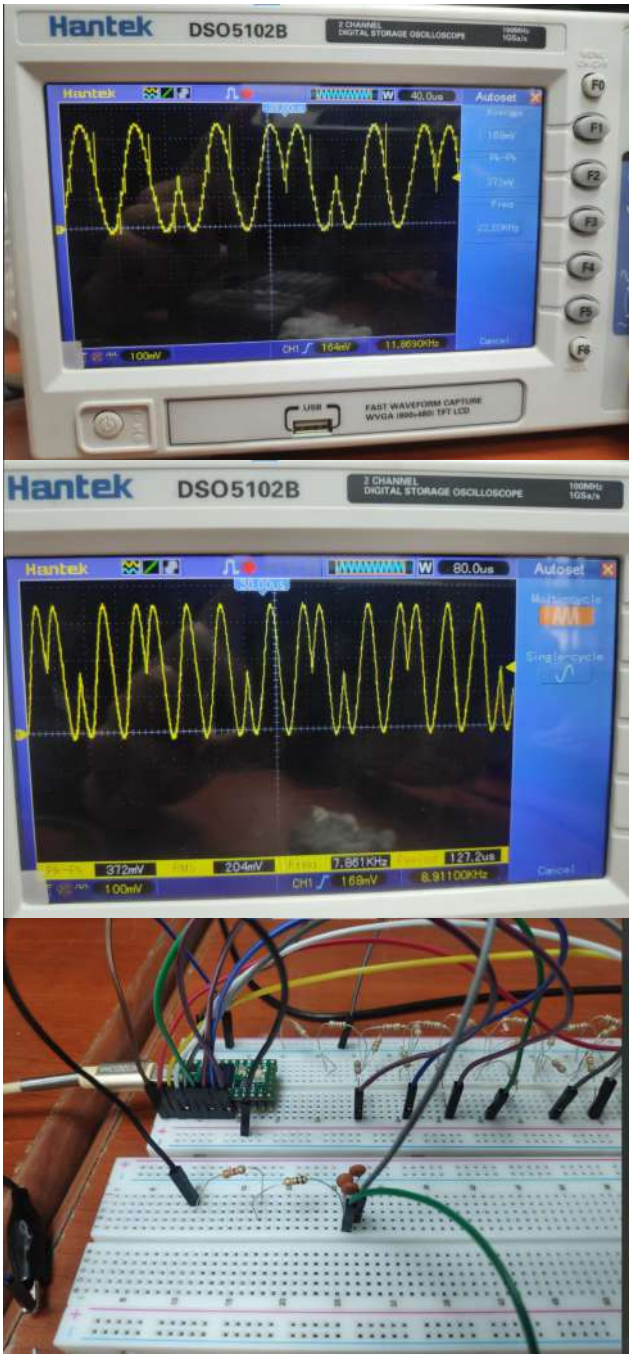


Figure 8. The DAC output at the top, the filter output in the middle, and the designed transmitter at the bottom.

in which $e^{-jx} = \cos(x) - j\sin(x)$, then (7) can be rewritten as

$$DFT = \sum_{n=0}^{3} S(n)\left(\cos\left(\frac{2\pi n}{4}\right) - j\sin\left(\frac{2\pi n}{4}\right)\right). \quad (8)$$

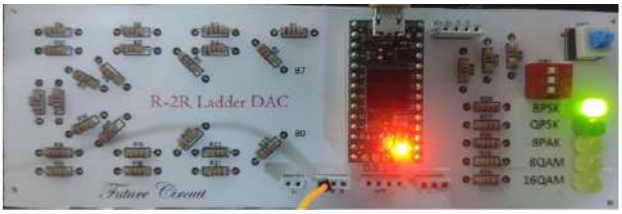


Figure 9. The PCB of the designed system.

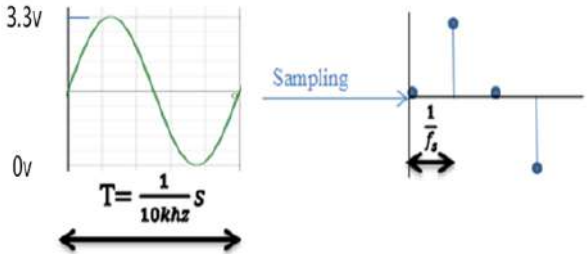


Figure 10. Synchronization method.

It is noteworthy that (8) results in a complex number as

$$DFT = I + jQ \quad (9)$$

Therefore, $tan^{-1}$ can be used to find the phase of the signal as

$$Phase = tan^{-1}\left(\frac{Q}{I}\right). \quad (10)$$

As $tan^{-1}$ gives the phase with the range of $-\pi/2$ to $\pi/2$ only, so we need to add additional parts to the code to find the phase, or we can use the *atan2* function instead, also the amplitude of the signal can be determined by calculating the absolute value of the signal's vector in the I-Q constellation diagram, using the following equation:

$$Amp. = \sqrt{I^2 + Q^2}. \quad (11)$$

However, because the sin is used as a reference for this paper to the x-axes, the DFT equation must be changed to be suitable for this process. This can be accomplished by representing the sin and cos by the x-axis and the y-axis, respectively. Furthermore, the negative sign of the y-axis is converted to positive, and that represents 90 degrees of rotation to the x-y plane. Then (8) becomes

$$DFT = \sum_{n=0}^{3} S(n)\left(\sin\left(\frac{2\pi n}{4}\right) + j\cos\left(\frac{2\pi n}{4}\right)\right). \quad (12)$$

The C language is used to evaluate (12), which is utilized then to obtain the phase value of the signal by assisting (10) and *atan2* function. The data can easily be demodulated according to modulation type after achieving these processing steps. The main challenge in our design is how to keep synchronization inside the microcontroller. This is for obtaining perfect signal recovery via exact estimation

of the phase. To overcome this issue a synchronous symbol has been added at the start of the transmission, so the receiver can know the start point of the first symbol by sensing the change in the channel and start to take samples in the correct position, the synchronous symbol can be a DC signal or a cos signal as shown in Figure 11. However,

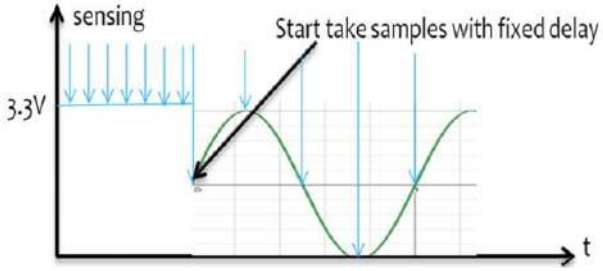


Figure 11. Sampling process explanation.

the delay between the expected and the actual samples is not perfect in each symbol due to a shift introduced in the sample position, which leads to an error in the detection of the phase after several symbols as shown in Figure 12. To

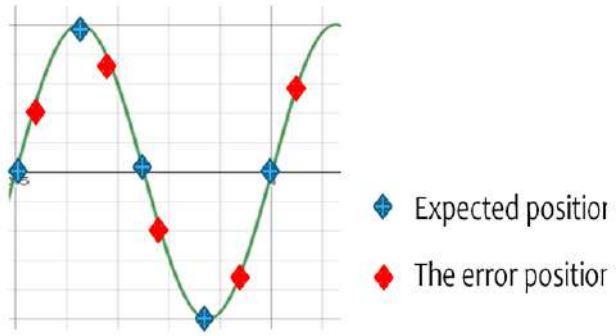


Figure 12. Samples shifting.

overcome this issue, symbol synchronous must be applied after a particular number of symbols as shown in Figure 13. The processing of the signal at the receiver is illustrated

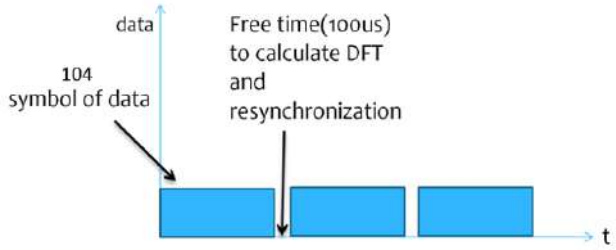


Figure 13. Samples shifting.

in Figure 14, which shows the implemented steps in a flow diagram. After adding all the required modifications to the receiver on the $\mu$C, synchronization is achieved and the designed receiver demodulates successfully the PSK,

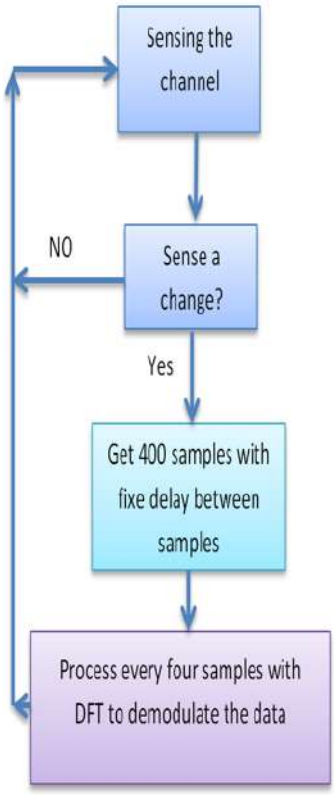


Figure 14. Receiver flow diagram.

QPSK, and 8PSK signals with 10KS/s. It is noteworthy that the 8PSK was not suitable with the 8-bit, i.e. byte size, and the 8PSK transfers 3 bits per symbol, so it needs an additional block in the code to select 3 bits for each symbol instead of an even number of bits for other modulation schemes. Moreover, Figure 15 illustrates the summary and the complete architecture of the SDR design presented in this paper, covering the entire path from the transmitter to the receiver.

## 5. RESULT ANALYSIS

After the data was demodulated and stored in the Teensy of the receiver, it was printed on the screen using a serial USP port and serial monitor tool that the Arduino IED offers as shown in Figure 16. 16. The data rate of one carrier of 10 KSps is obtained as 10kbit for PSK, 20Kbits for QPSK, and 30Kbit for 8PSK. Furthermore, the modulation type can be changed for both the transmitter and the receiver. Moreover, after that BER against the carrier-to-noise ratio (CNR) is calculated for the designed real-time system, the obtained results has been compered with the simulation results obtained by a Matlab code in the presence of additive while Gaussian noise (AWGN) and by using 10 Kbits of data, both results demonstrated exact-close match as shown in Figure 17. The results show that the SDR receiver works perfectly with high synchronization, and it achieved the same result as the simulation for PSK and QPSK, Moreover,

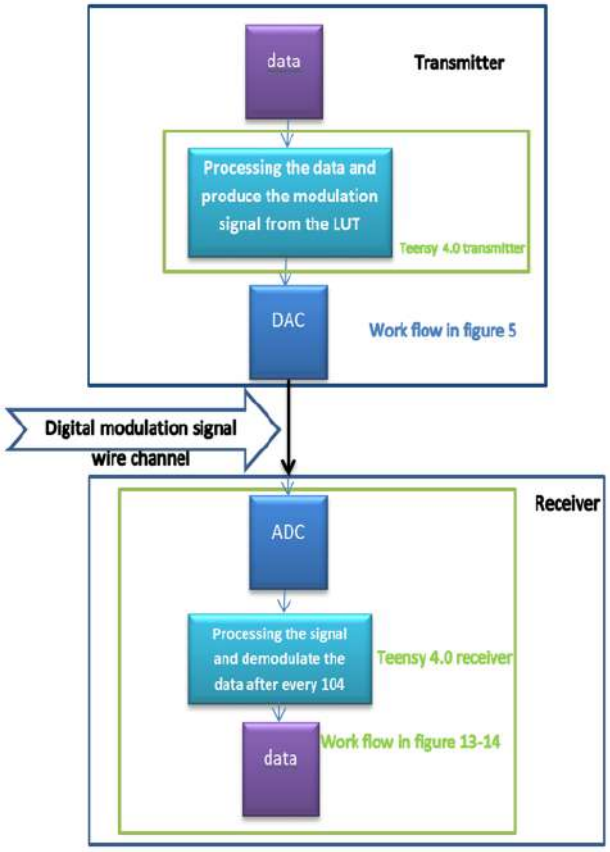


Figure 15. The entire architecture of the designed real-time system.

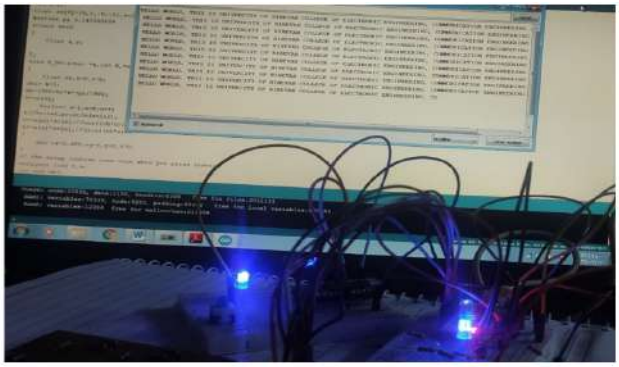

Figure 16. Demodulated data.

from practical experience, a transfer speed of 100 kb/s is achieved using QPSK modulation with symbol rate of about 50kbps. Also from the experience the transmitter can reach a speed of up to 400 KSps when 16QAM is chosen. For this modulation scheme, the system can transmit up to 400KS/s*4bits=1.6Mbps, and the frequency can be increased by decreasing the number of samples per period, which is assumed 25 samples per period in the proposed design. This makes the LPF design much easier with lower complexity. Additionally, the data rate can be

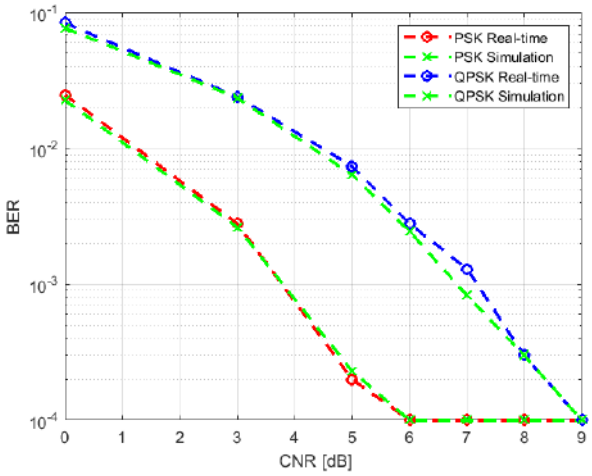


Figure 17. The BER against CNR for real-time and simulation of PSK and QPSK.

increased using a multi-carrier system, and the receiver speed can be increased by taking three samples per symbol instead of four. The receiver needs about 50$\mu$s to implement the DFT for the 104 symbols, and the internal ADC of Teensy 4.0 needs 3$\mu$s for every sample at a maximum rate of 333 KS/s, which theoretically can demodulate signals up to 83KHz by using this method if four samples per symbol are considered, not three per symbol. On the other side, the synchronization still needs an additional symbol duration. The maximum available frequency is 83 KHz, and the period of one symbol is $t = 1/83KHz = 12\mu$s. Thus, DFT needs 50$\mu$s for processing plus 50$\mu$s as a guard interval which means that 100$\mu$s is required for processing 104 symbols, i.e. the processing time is equal to the time intervals of 8 symbols.

Therefore, the number of symbols needed for processing is $100\mu s/12\mu s = 8.3$ symbol for every 104 symbols of data, from these results, we can conclude that the maximum symbol rate that can be obtained from the designed system is 83KSps-(83KSps/104 $*$ 8.3) =76.4KSps of data, which means that it is about 300kbit if 16QAM used. For QAM, the same method can be applied; however, after detecting the phase, it is also necessary to determine the amplitude using (10). This ensures the correct mapping of symbols for accurate data demodulation in ideal environment, but in real world scenarios for QAM, the $\mu$C must monitor the power level of the attenuated signal to choose a reference power level to demodulate QAM signal correctly. It is noteworthy that the receiver speed can be increased by adding an external ADC or by decreasing the number of resynchronize symbols, however, this data rate is more than the real-time digital voice needed. This method of synchronization of the symbol can be applied also to a multi-carrier system like OFDM which we will need only to synchronize the symbol's length not all the subcarriers.

## 6. Conclusions

The $\mu$Cs make the design of digital communication systems flexible but limited by the range of the clock speed of the processor. The design can be changed according to the requirements of the systems and applications. This paper has considered designing a multi-real-time modulator for a single carrier based on an $\mu$C. The signal is digitally modulated over different modulation schemes at the transmitter by utilizing a LUT model that stores all probable symbols of any modulation scheme in the Teensy microcontroller. On the other hand, at the receiver, a DSP algorithm, via utilizing a single carrier discrete Fourier transform (DFT), has been proposed and implemented. The detection by using the proposed method relies on phase detection of the symbols, and it successfully modulates the data of 10Ks/s, because of the flexibility of the $\mu$C a synchronous symbol that has been added to the signal to confirm the correct demodulation. There are a wide number of ideas that can be applied to this designed system, in which the transmitter can be used as a lab board or a flexible real-time transmitter for signal carriers or multi-carrier systems like OFDM with 400KS/s speed. Moreover, the designed receiver can be employed to receive signals with a suitable speed for real-time digital voice. The maximum assumption speed that can be obtained from our prospered system was 76.4Ks/s for four samples per symbol. This rate can be extended to be suitable for multi-modulation schemes. The ability to implement a receiver for QAM signal can be investigated as well by applying the same idea. The designed system, with the transmitter and receiver, can be utilized also as a half-duplex connection with multiple devices. Besides, it can be applied to a multi-carrier system like OFDM or make it automatically discover the bit rate and the scheme of modulation, and deceptively change the modulation according to the received data or the level of power. Furthermore, it can be worked as a two-way half-duplex communication system, and error correction bits like Hamming code can be added and calculated in the re-synchronize symbol time within the spare time that is added in the designed system which is about 50us. Also, the $\mu$C can be programmed to compere the received phase with the nearest symbol point of modulation to calculate the error vector of the signal. Moreover, this microcontroller, with a 600MHz clock speed, can handle a maximum data rate that can be suitable for real-time digital voice, also it is suggested to calculate the maximum rang of transfer data in future work.

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